IN THE CLAIMS

1. (Previously presented) A single-die integrated circuit for switching among a plurality of transmission ports and a plurality of receiver ports, comprising:

a transmitter switching section having a plurality of transmission ports, the transmitter switching section operable to switch a selected one of the plurality of transmission ports to a transmission node; and

a receiver switching section having a plurality of receiver ports, the receiver switching section operable to switch a selected one of the plurality of receiver ports to the transmission node, wherein the receiver switching section includes at least two cascaded stages, a first cascaded stage controllable to switch the transmission node to a receiver node, and a second cascaded stage controllable to switch the receiver node to a selected one of the plurality of receiver ports.

2. (Cancelled)

3. (Original) The integrated circuit of claim 1, and further comprising an antenna port coupled to the transmission node.

4. (Previously presented) The integrated circuit of claim 1, wherein, for each transmission port, the transmitter switching section includes a series field effect transistor (FET) switching topology comprising a plurality of transistors with their current paths coupled in series between an associated transmission port and the

transmission node.

5. (Cancelled)

6. (Previously presented) The integrated circuit of claim 4, wherein at least one of the FET switching topologies includes at least one FET having a plurality of contiguous source regions interdigitated with a plurality of contiguous drain regions, and a sinuous gate formed to wind between the source regions and the drain regions.

7. (Previously presented) A single-die multiband switch for wireless communication, comprising:

an antenna port;

a plurality of transmitter ports, for each transmitter port a switching topology operable to switch the last said transmitter port to the antenna port; and

a plurality of receiver ports, for each receiver port a switching topology operable to switch the last said receiver port to the antenna port;

wherein at least one of the switching topologies comprises a plurality of field effect transistors having their current paths coupled in series between an associated transmission port and the antenna port, a control signal for the at least one switching topology controlling the at least one switching topology to selectively connect or isolate a respective transmitter port from the antenna port.

8. (Cancelled)

9. (Original) The switch of claim 7, wherein at least one of the switching topologies comprises at least one interdigitated field effect transistor having a plurality of elongated contiguous drain regions, a plurality of elongated contiguous source regions interdigitated with the drain regions, an elongated sinuous channel region spacing apart the drain regions from the source regions, and a gate overlying the channel region to switch the interdigitated field effect transistor between an ON and an OFF state.

10. (Original) The switch of claim 7, wherein the die has an area, the transmitter port switching topologies occupying an area on the die which is substantially larger than the receiver port switching topologies.

11. (Original) The switch of claim 7, and further including at least one multiple-stage switching topology, a first stage of the multiple-stage switching topology selectively connecting or isolating the antenna port from the multiple-stage switching topology, a last stage of the multiple-stage switching topology selectively connecting or isolating a plurality of other ports from the multiple-stage switching topology.

12. (Previously presented) The switch of claim 11, wherein the other ports are receiver ports.

13. (Previously presented) The switch of claim 12, wherein the last stage includes, for each receiver port, a signal path FET having a current path controllable to connect the receiver port to an intermediate node, the first stage operable to connect the intermediate node to the antenna port.

14. (Original) A single-die transmitter/receiver integrated switching circuit, comprising:

a plurality of transmitter ports;

a plurality of receiver ports;

at least one antenna port;

a plurality of integrated circuit switching elements controllable to connect one of the transmitter ports or one of the receiver ports to the antenna port while isolating the remaining ones of the transmitter and receiver ports from the antenna port, at least one of the plurality of transmitter ports and the plurality of receiver ports being at least three in number, at least some of the integrated circuit switching elements arranged in cascaded fashion in order to reduce signal insertion loss.

15. (Original) The integrated switching circuit of claim 14, wherein there are at least three receiver ports, any one receiver port selectably switched to be connected to the antenna port through at least two cascaded stages of integrated circuit switching elements.

16. (Original) The integrated switching circuit of claim 14, wherein the integrated circuit switching elements are field effect transistors.

17. (Previously presented) A method of switching one of a plurality of transmitters and a plurality of receivers to a transmitter/receiver antenna, comprising the steps of:

connecting each transmitter to a respective one of a plurality of transmitter ports formed on a single integrated circuit die;

connecting each receiver to a respective one of a plurality of receiver ports formed on the die;

controlling a selected one of a plurality of switching topologies each associated with a respective one of the transmitter and receiver ports to connect a respective selected one of the transmitter and receiver ports to an antenna port formed on the die;

controlling other ones of the switching topologies to isolate others of the transmitter and receiver ports from the antenna port;

arranging at least some of the switching topologies in cascaded stages including a first stage coupled to the antenna port and a last stage coupled to a plurality of the transmitter or receiver ports;

connecting a selected one of the transmitter or receiver ports to the antenna port by switching on the first stage and switching on a switch associated with the selected one of the transmitter or receiver ports wherein the switch

associated with the selected one of the transmitter or receiver ports is a portion of the last stage; and

switching off the remaining switching topologies and other switches in the last stage.

18. (Cancelled)

19. (Previously presented) The method of claim 17, wherein the step of controlling a selected one of the switching topologies includes the step of switching a plurality of series-connected switching transistors to an ON state.

20. (Previously presented) The integrated circuit of claim 1 wherein the first cascaded stage comprises at least one first transistor having a current path coupled between the transmission node and an intermediate node and the second cascaded stage comprising at least one second transistor for each of the receiver ports, said transistor of each of the receiver ports having a current path coupled between the intermediate node and the corresponding receiver node, wherein the at least one transistor has a gate perimeter that is about twice the gate perimeter of at least one of the second transistors.